REMARKS

Initially, Applicants wish to thank the Examiner for the detailed Final Office Action and for the Notice of References Cited. Applicants note that the Examiner still has not indicated consideration the Information Disclosure Statement filed on September 15, 2006, which the Examiner asserts fails to comply with 37 C.F.R. §1.98(a)(1). As previously discussed, the documents cited in the Information Disclosure Statement filed on September 15, 2006 were earlier submitted for the Examiner's consideration with the Information Disclosure Statement filed on July 21, 2006 (as noted on page 2 of the Information Disclosure Statement filed on September 15, 2006) *and* the Examiner acknowledged consideration of each of the documents cited in the Information Disclosure Statement filed on July 21, 2006. Thus, unless indicated otherwise in the next Official communication, Applicants conclude that the Examiner considered the materials noted in the September 15, 2006 Information Disclosure Statement, said documents having earlier been considered in the July 21, 2006 Information Disclosure Statement.

In the outstanding Final Office Action, claims 1, 2 and 6-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI in view of PALANCA (U.S. Patent No. 6,202,129). Claims 3 and 4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI in view of PALANCA as applied to claim 2 above, and further in view of PETTEY (U.S. Patent No. 6,021,480).

Upon entry of the present amendment, independent claims 1 and 10 and dependent claim 9 will have been amended and dependent claim 6 will have been cancelled. Independent claims 1 and 10 will have been amended to recite features similar to features previously recited in now-cancelled claim 6, support for which may be found at, for example, paragraph [0145] of the published application (*i.e.*, U.S. Patent Application Publication No. 2008/168232). Dependent claims 2 and 9 will have been amended to address a noted informality. The amendments to

independent claims 1 and 10 and dependent claims 2 and 9 and the cancellation of dependent claim 6 should not be considered an indication of Applicants' acquiescence as to any of the outstanding rejections. Rather, Applicants have amended independent claims 1 and 10 and dependent claims 2 and 9 and cancelled dependent claim 6 to advance the prosecution and to obtain an early allowance of the present application.

Applicants respectfully traverse the rejection of claims 1, 2 and 6-10 under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI in view of PALANCA and the rejection of claims 3 and 4 under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI in view of PALANCA as applied to claim 2 above, and further in view of PETTEY. In this regard, the Examiner asserts column 4, lines 12-15 and 23-31, column 3, lines 36-37 as well as Figures 1 and 2 of ARIMILLI as teaching the claimed modifier and selector. Applicants respectfully submit that ARIMILLI discloses a cache memory having a programmable cache replacement scheme. The Examiner acknowledges that ARIMILLI fails to disclose or render obvious that a selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present, as recited in Applicants' independent claim 1, and relies on PALANCA as teaching these noted features of Applicants' independent claim 1.

Applicants submit that cache 50 disclosed in PALANCA includes an array of least recently used (LRU) lock bits 70_0 -70_n which indicates whether any of the ways 52, 54, 56 and 58 within a given set contain data that should not pollute the cache 50 (*i.e.*, data with *infrequent* usage). More particularly, the LRU lock bits 70_0 -70_n disclosed by PALANCA are submitted to indicate whether the corresponding cache data is streaming or non-temporal and accordingly, should be the first entry to be replaced upon a cache miss to the corresponding set (*see e.g.*, column 6, lines 16-20 of PALANCA). The Examiner further asserts that an LRU lock bit disclosed by PALANCA is analogous to the claimed oldest-order flag. However, Applicants

respectfully submit that the LRU lock bits disclosed by PALANCA merely indicate infrequent data usage, but not *least frequent data usage, which the claimed oldest-order flag specifies*. Further, it is submitted that PALANCA fails to disclose or render obvious at least a cache entry having an oldest-order flag attached at least insofar as there is one LRU lock bit 70 for the entire set, but not for each and every way in the set (*see e.g.*, Figure 3 of PALANCA). Accordingly, Applicants respectfully submit that the combination of ARIMILLI and PALANCA set forth by the Examiner does not disclose *an oldest-order flag*, let alone selecting a cache entry to be replaced when a cache miss occurs and a cache entry having an oldest-order flag attached is present, as specified in Applicants' independent claim 1.

Applicants' amended independent claim 1 recites, *inter alia*, that the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset. Applicants amended independent claim 1 further recites, *inter alia*, a selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present. The amended features of Applicants' independent claim 1 are similar to features previously recited in now-cancelled dependent claim 6. The Examiner asserts portions of PALANCA in column 5, lines 41-43 and lines 59-62 as well as element 60 of Figure 3 as teaching that a cache entry has, as the order data, a 1-bit order flag that indicates whether the access order is old or new, and that a selector selects as the cache entry to be replaced, the cache entry in which the order flag indicates old when the cache entry having the oldest-order flag attached is not present. Applicants submit that PALANCA discloses a cache 50 that includes an array of LRU bits 60_0-60_n, each of which points to the way within a set with the least recently used data. Applicants' amended independent claim 1 clarifies that the 1-bit

order flag indicates whether an access has occurred since the cache entries in the cache memory were reset (*i.e.*, each reset to each indicate that no access had occurred). According to an aspect of the present application, the claimed 1-bit order flag is concurrently enabled for more than one cache entry in a cache memory. In contrast, the LRU bits 60_0-60_n disclosed by PALANCA would *not* appropriately indicate a cache entry that had been accessed since the cache entries had been reset, if the cache entry had not been accessed earliest after the reset. Rather, Applicants submit that each of the LRU bits 60_0-60_n disclosed by PALANCA only points to *a single way within a set with the least recently used data*.

Applicants respectfully submit that the combination of ARIMIILLI in view of PALANCA set forth by the Examiner fails to disclose or renders obvious that the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset, as recited in Applicants' independent claim 1. Further, Applicants respectfully submit that the combination of ARIMIILLI in view of PALANCA set forth by the Examiner fails to disclose or renders obvious a selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag attached is not present, as recited in Applicants' amended independent claim 1.

In view of the above, Applicants respectfully submit that independent claim 1 is allowable over ARIMILLI in view of PALANCA for at least the reasons set forth above.

In addition, the method of independent claim 10 is submitted to be allowable for reasons similar to those noted above with respect to independent claim 1 in addition to reasons related to its own recitations.

Applicants respectfully submit that each of dependent claims 2 and 7-9 are allowable at least because they depend, directly or indirectly, from independent claim 1 which Applicants submit has been shown to be allowable. Each of dependent claims 2 and 7-9 are also believed to recite further patentable subject matter. Applicants submit that the cancellation of dependent claim 6 renders moot the rejection of dependent claim 6 over ARIMILLI in view of PALANCA. Further, arguments made above with respect to the rejection of independent claim 1 are applicable hereto insofar as each of claims 3 and 4 which depend from independent claim 1. Applicants respectfully submit that each of dependent claims 3 and 4 are also believed to recite further patentable subject matter and that PETTEY fails to cure the deficiencies noted above with respect to the combination of ARIMILLI in view of PALANCA set forth by the Examiner. As such, allowance of the dependent claims is deemed proper for at least the same reasons noted for the independent claims upon which they depend, in addition to reasons related to their own recitations.

Accordingly, reconsideration and withdrawal of the rejection of claims 1, 2 and 6-10 under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI in view of PALANCA and the rejection of claims 3 and 4 under 35 U.S.C. §103(a) as being unpatentable over ARIMILLI in view of PALANCA as applied to claim 2 above, and further in view of PETTEY is respectfully requested.

At least in view of the herein contained amendments and remarks, Applicants respectfully request reconsideration and withdrawal of each of the outstanding rejections, together with an indication of the allowability of all pending claims, in due course. Such action is respectfully requested and is believed to be appropriate and proper.

Applicants note that this Response is being submitted after a Final Office Action has been mailed. Applicants respectfully request entry and consideration of this Response, including the

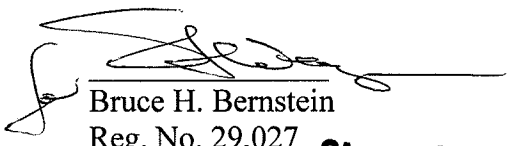
amendments provided herein, and believe such entry and consideration is proper. Applicants also respectfully request the Examiner to reconsider and to withdraw all of the outstanding ejections made in the outstanding Final Office Action, and to allow the application to mature to a U.S. letters patent. Applicants believe that such action is now proper and called for, for at least the reasons provided below.

Applicants recognize that Applicants cannot, as a matter of right, amend any finally rejected claims. However, Applicants also recognize that any amendment that will place the application either in condition for allowance or in better form for appeal may be entered. Applicants respectfully submit that entry and consideration of this Response, including amendments provided herein, is appropriate and timely.

Should an extension of time be necessary to maintain the pendency of this application, including any extensions of time required to place the application in condition for allowance by an Examiner's Amendment, the Commissioner is hereby authorized to charge any additional fee to Deposit Account No. 19-0089.

Should the Examiner have any questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully Submitted,
Hazuki OKABAYASHI et al.



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